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EXAMINER	
KRAIG, WILLIAM F	
ART UNIT	**PAPER NUMBER**
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SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/26/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/790,211	AOKI, TAKAAKI	
	Examiner	Art Unit	
	William Kraig	2815	

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 January 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2 and 4-25* is/are pending in the application.

4a) Of the above claim(s) *17-25* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2 and 4-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date *10/5/2006*.
4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. The Examiner's objections to the claims are withdrawn in light of the Applicant's amendments to the claims dated 12/14/2006.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 5, 7, 11, and 13 rejected under 35 U.S.C. 103(a) as being unpatentable over Aoki et al. (U.S. Patent # 6469345) in view of Jin et al. (U.S. Patent # 6350665) and further in view of Yu et al. (U.S. Patent # 6784101) and further in view of Currie et al. ("Carrier Mobilities and Process Stability of Strained Si n- and p-mosfets on SiGe Virtual Substrates", J. Vac. Sci. Tech. B 19(6), Nov/Dec 2001).

Regarding claim 1, Aoki et al. discloses a method for manufacturing a semiconductor device comprising the steps of:

forming a trench (6) having an inner wall (inner wall of trench is covered with insulation film (7a) in Fig. 2B) in a substrate (1, 2, 3);

forming an insulation film (Fig. 2C (7a)) on the inner wall of the trench;

forming a conductive film (Fig. 2G, (8)) in the trench on the insulation film;

wherein the substrate (Aoki et al., Fig. 2H (1, 2, 3)) is made of silicon (Aoki et al., Col. 2, Lines 48-50).

Aoki et al., however, fails to disclose annealing the substrate at an annealing temperature after the step of forming the conductive film.

Fig. 5A of Jin et al., however, teaches the annealing (516) of a substrate at an annealing temperature after the formation of a conductive gate electrode (502) (Col. 12, Lines 43-54).

It would have been obvious to one of ordinary skill in the art to incorporate the annealing step of Jin et al. into the method of Aoki et al. The ordinary artisan would have been motivated to modify the method of Aoki et al. in the above manner for the purpose of repairing lattice damages produced by previous ion-implantation steps (Jin et al., Col. 12, Lines 43-53).

Aoki et al., and Jin et al., however, fail to disclose the annealing temperature being, specifically, higher than 1150 degrees Celsius and equal to or less than 1200 degrees Celsius.

Yu et al., however, teaches an RTA process (Yu et al., Col. 5, Lines 24-35) wherein the annealing temperature is equal to 1200 degrees Celsius (Yu et al., Col. 4, Lines 24-35).

It would have been obvious to one of ordinary skill in the art to incorporate the annealing temperature of Yu et al. into the process of Aoki et al. and Jin et al. One of ordinary skill in the art would have been motivated to increase the annealing temperature of Aoki et al. and Jin et al. in the above manner for the purpose of

minimizing dopant diffusion while maximizing implantation-induced defect removal (Currie et al., Page 2276, Col. 1, Lines 7-12).

Regarding the limitations "for improvement of reliability of the insulation film" and "so that a damage in the insulation film is removed at the annealing temperature", it is not necessary for the reference to disclose that the process of the reference is performed to achieve the same goals as applicant or to obtain the same advantages recognized by applicant. It is sufficient that the process suggested by the reference alone or in combination with the remaining references is encompassed by the instant claims.

Regarding claim 5, Aoki et al., Jin et al., Yu et al. and Currie et al. disclose the method according to claim 1, wherein the conductive film is made of doped poly crystalline silicon (Aoki et al., Col. 3, Lines 7-8), and wherein the insulation film is made of silicon oxide and silicon nitride (Aoki et al., Col. 2, Lines 57-62).

Regarding claim 7, Aoki et al., Jin et al., Yu et al. and Currie et al. disclose the method according to claim 1,

wherein the insulation film (Aoki et al., Fig. 2C (7a)) includes an oxide-nitride-oxide film (Aoki et al., Fig. 2H (7a, 7b, 7c)) and upper (Aoki et al., Fig. 2H (7d)) and lower oxide films (Aoki et al., Fig. 2H (7e)),

wherein the trench (Aoki et al., Fig. 2B (6)) includes a sidewall (Aoki et al., Fig. 2H (side walls of trench (6), having oxide film (7a) disposed thereon)) and

upper (Aoki et al., Fig. 2H (upper portion of trench (6), having oxide film (7d) disposed thereon)) and lower portions (Aoki et al., Fig. 2H (lower portion of trench (6), having oxide film (7e) disposed thereon)),

wherein the oxide-nitride-oxide film (Aoki et al., Fig. 2H (7a, 7b, 7c)) is disposed on the sidewall of the trench (Aoki et al., Fig. 2H (side walls of trench (6), having oxide film (7a) disposed thereon)), the upper oxide film (Aoki et al., Fig. 2H (7d)) is disposed on the upper portion of the trench (Aoki et al., Fig. 2H (upper portion of trench (6), having oxide film (7d) disposed thereon)), and the lower oxide film (Aoki et al., Fig. 2H (7e)) is disposed on the lower portion of the trench (Aoki et al., Fig. 2H (lower portion of trench (6), having oxide film (7e) disposed thereon)),

wherein the oxide-nitride-oxide film (Aoki et al., Fig. 2H (7a, 7b, 7c)) includes a silicon oxide film (Aoki et al., Fig. 2H (7a)), a silicon nitride film (Aoki et al., Fig. 2H (7b)) and another silicon oxide film (Aoki et al., Fig. 2H (7c)) (Aoki et al., Col. 2, Lines 57-62), and

wherein the upper (Aoki et al., Fig. 2H (7d)) and lower (Aoki et al., Fig. 2H (7e)) oxide films are made of silicon oxide (Aoki et al., Col. 2, Lines 66-67).

Regarding claim 11, Aoki et al., Jin et al., Yu et al. and Currie et al. disclose a method for manufacturing a semiconductor device comprising the steps of:

forming a trench (Aoki et al., Fig. 2H (6)) having an inner wall (Aoki et al. (inner wall of trench is covered with insulation film (7a) in Fig. 2B)) in a substrate (Aoki et al., Fig. 2H (1, 2, 3));

forming an insulation film (Aoki et al., Fig. 2H (7a, 7b, 7c)) on the inner wall of the trench;

forming a gate electrode (Aoki et al., Fig. 2H (8)) in the trench on the insulation film;

implanting an impurity into the substrate with using the gate electrode as a mask after the step of forming the gate electrode (Jin et al., Col. 10, Lines 17-25) (Jin et al., Fig. 5A (502));

performing a thermal diffusion process for diffusing the impurity so that a source region adjacent to the trench (Aoki et al., Fig. 2H (4)) and disposed on a surface of the substrate is formed (Aoki et al., Col. 3, Lines 34-38); and

annealing (Jin et al., Fig. 5A (516)) the substrate at an annealing temperature after the step of forming the conductive film (Jin et al., Fig. 5A (502)) (Jin et al., Col. 12, Lines 43-54),

wherein the substrate (Aoki et al., Fig. 2H (1, 2, 3)) is made of silicon (Aoki et al., Col. 2, Lines 48-50), and

wherein the annealing temperature is equal to 1200 degrees Celsius (Yu et al., Col. 4, Lines 24-35).

Regarding the limitations "for improvement of reliability of the insulation film" and "so that a damage in the insulation film is removed at the annealing temperature", it is

not necessary for the reference to disclose that the process of the reference is performed to achieve the same goals as applicant or to obtain the same advantages recognized by applicant. It is sufficient that the process suggested by the reference alone or in combination with the remaining references is encompassed by the instant claims.

Regarding claim 13, Aoki et al., Jin et al., Yu et al. and Currie et al. disclose the method according to claim 11,

wherein the insulation film (Aoki et al., Fig. 2C (7a)) includes an oxide-nitride-oxide film (Aoki et al., Fig. 2H (7a, 7b, 7c)) and upper (Aoki et al., Fig. 2H (7d)) and lower oxide films (Aoki et al., Fig. 2H (7e)),

wherein the trench (Aoki et al., Fig. 2B (6)) includes a sidewall (Aoki et al., Fig. 2H (side walls of trench (6), having oxide film (7a) disposed thereon)) and upper (Aoki et al., Fig. 2H (upper portion of trench (6), having oxide film (7d) disposed thereon)) and lower portions (Aoki et al., Fig. 2H (lower portion of trench (6), having oxide film (7e) disposed thereon)),

wherein the oxide-nitride-oxide film (Aoki et al., Fig. 2H (7a, 7b, 7c)) is disposed on the sidewall of the trench (Aoki et al., Fig. 2H (side walls of trench (6), having oxide film (7a) disposed thereon)), the upper oxide film (Aoki et al., Fig. 2H (7d)) is disposed on the upper portion of the trench (Aoki et al., Fig. 2H (upper portion of trench (6), having oxide film (7d) disposed thereon)), and the

lower oxide film (Aoki et al., Fig. 2H (7e)) is disposed on the lower portion of the trench (Aoki et al., Fig. 2H (lower portion of trench (6), having oxide film (7e) disposed thereon)),

wherein the oxide-nitride-oxide film (Aoki et al., Fig. 2H (7a, 7b, 7c)) includes a silicon oxide film (Aoki et al., Fig. 2H (7a)), a silicon nitride film (Aoki et al., Fig. 2H (7b)) and another silicon oxide film (Aoki et al., Fig. 2H (7c)) (Aoki et al., Col. 2, Lines 57-62), and

wherein the upper (Aoki et al., Fig. 2H (7d)) and lower (Aoki et al., Fig. 2H (7e)) oxide films are made of silicon oxide (Aoki et al., Col. 2, Lines 66-67).

3. Claims 2, 4, 6, 8-10, 14, and 15 rejected under 35 U.S.C. 103(a) as being unpatentable over Aoki et al. in view of Jin et al., further in view of Yu et al., further in view of Currie et al. and further in view of Inagawa et al. (U.S. Patent # 6455378).

Regarding claim 2, Aoki et al., Jin et al., Yu et al. and Currie et al. disclose the method according to claim 1, further comprising the step of:

forming a source region (Aoki et al., Fig 2B, (4)) having a contact surface between the source region and the substrate (Aoki et al., Fig. 2B, (contact surface is bottom surface of source region (4))), which is disposed near the trench (Aoki et al., Fig. 2B (6)) and is almost parallel to the substrate (see Fig. 2B),

wherein the insulation film (Aoki et al., Fig. 2C (7a)) includes an oxide-nitride-oxide film (Aoki et al., Fig. 2H (7a, 7b, 7c)) and upper (Aoki et al., Fig. 2H (7d)) and lower oxide films (Aoki et al., Fig. 2H (7e)),

wherein the conductive film (Aoki et al., Fig. 2H (8)) in the trench provides a gate electrode (Aoki et al., Col. 4, Lines 26-28),

Aoki et al., Jin et al., Yu et al. and Currie et al., however, fail to disclose the gate electrode including a canopy for covering the upper oxide film so that the gate electrode has a T-shaped cross section, and the canopy of the gate electrode having an edge, which is disposed at a predetermined distance from an edge of an opening of the trench, and the predetermined distance being predetermined not to prevent the source region from forming.

Fig. 16(c) of Inagawa et al. teaches a gate electrode (3(3b)) including a canopy for covering the upper oxide film so that the gate electrode has a T-shaped cross section (See Fig. 16(c)), the canopy of the gate electrode having an edge (edge of gate electrode (3(3b)) coincident with layer (2b)), said edge being disposed at a predetermined distance (distance between edge of gate electrode (3(3b)) coincident with layer (2b) and edge of trench opening (see Fig. 16(c))) from an edge of an opening of the trench, wherein the predetermined distance (distance between edge of gate electrode (3(3b)) coincident with layer (2b) and edge of trench opening (see Fig. 16(c))) is predetermined not to prevent the source region (6) from forming (Col. 11, Lines 59-60).

It would have been obvious to one of ordinary skill in the art to incorporate the gate electrode of Inagawa et al. into the method of Aoki et al., Jin et al., Yu et al. and Currie et al. One of ordinary skill in the art would have been motivated to modify Aoki et al., Jin et al., Yu et al. and Currie et al. in the above manner for the purpose of having more control over the depth of the source region (Inagawa et al., Col. 11, Lines 54-60).

Regarding claim 4, Aoki et al., Jin et al., Yu et al., Currie et al. and Inagawa et al. disclose the method according to claim 1, further comprising the step of:

forming a source region (Aoki et al., Fig 2B, (4)) having a contact surface between the source region and the substrate (Aoki et al., Fig. 2B, (contact surface is bottom surface of source region (4))), which is disposed near the trench (Aoki et al., Fig. 2B (6)) and is almost parallel to the substrate (see Fig. 2B),

wherein the insulation film (Aoki et al., Fig. 2C (7a)) includes an oxide-nitride-oxide film (Aoki et al., Fig. 2H (7a, 7b, 7c)) and upper (Aoki et al., Fig. 2H (7d)) and lower oxide films (Aoki et al., Fig. 2H (7e)),

wherein the conductive film (Aoki et al., Fig. 2H (8)) in the trench provides a gate electrode (Aoki et al., Col. 4, Lines 26-28),

wherein the gate electrode includes a canopy for covering the upper oxide film so that the gate electrode has a T-shaped cross section, and the canopy of the gate electrode has an edge, which is disposed at a predetermined distance from an edge of an opening of the trench, and the predetermined distance being

predetermined not to prevent the source region from forming (Fig. 16(c) of Inagawa et al. teaches a gate electrode (3(3b)) including a canopy for covering the upper oxide film so that the gate electrode has a T-shaped cross section (See Fig. 16(c)), the canopy of the gate electrode having an edge (edge of gate electrode (3(3b)) coincident with layer (2b)), said edge being disposed at a predetermined distance (distance between edge of gate electrode (3(3b)) coincident with layer (2b) and edge of trench opening (see Fig. 16(c))) from an edge of an opening of the trench, wherein the predetermined distance (distance between edge of gate electrode (3(3b)) coincident with layer (2b) and edge of trench opening (see Fig. 16(c))) is predetermined not to prevent the source region (6) from forming (Col. 11, Lines 59-60))

Regarding claim 6, Aoki et al., Jin et al., Yu et al., Currie et al. and Inagawa et al. disclose the method according to claim 5, further comprising the step of:

forming a source region (Aoki et al., Fig 2B, (4)) having a contact surface between the source region and the substrate (Aoki et al., Fig. 2B, (contact surface is bottom surface of source region (4))), which is disposed near the trench (Aoki et al., Fig. 2B (6)) and is almost parallel to the substrate (see Fig. 2B),

wherein the insulation film (Aoki et al., Fig. 2C (7a)) includes an oxide-nitride-oxide film (Aoki et al., Fig. 2H (7a, 7b, 7c)) and upper (Aoki et al., Fig. 2H (7d)) and lower oxide films (Aoki et al., Fig. 2H (7e)),

wherein the conductive film (Aoki et al., Fig. 2H (8)) in the trench provides a gate electrode (Aoki et al., Col. 4, Lines 26-28),

wherein the gate electrode (Inagawa et al., Fig. 16(c) (3(3b))) includes a canopy for covering the upper oxide film so that the gate electrode has a T-shaped cross section (Inagawa et al., Fig. 16(c)),

wherein the canopy of the gate electrode has an edge (Inagawa et al., Fig. 16(c) (edge of gate electrode (3(3b)) coincident with layer (2b))), said edge being disposed at a predetermined distance (Inagawa et al., Fig. 16(c) (distance between edge of gate electrode (3(3b)) coincident with layer (2b) and edge of trench opening (see Fig. 16(c)))) from an edge of an opening of the trench,

wherein the predetermined distance (Inagawa et al., Fig. 16(c) (distance between edge of gate electrode (3(3b)) coincident with layer (2b) and edge of trench opening (see Fig. 16(c)))) is predetermined not to prevent the source region (Inagawa et al., Fig. 16(c) (6)) from forming (Inagawa et al., Col. 11, Lines 59-60).

Regarding claim 8, Aoki et al., Jin et al., Yu et al., Currie et al. and Inagawa et al. disclose the method according to claim 7, further comprising the step of:

forming a source region (Aoki et al., Fig 2B, (4)) having a contact surface between the source region and the substrate (Aoki et al., Fig. 2B, (contact surface is bottom surface of source region (4))), which is disposed near the

trench (Aoki et al., Fig. 2B (6)) and is almost parallel to the substrate (see Fig. 2B),

wherein the conductive film (Aoki et al., Fig. 2H (8)) in the trench provides a gate electrode (Aoki et al., Col. 4, Lines 26-28),

wherein the gate electrode (Inagawa et al., Fig. 16(c) (3(3b))) includes a canopy for covering the upper oxide film so that the gate electrode has a T-shaped cross section (Inagawa et al., Fig. 16(c)),

wherein the canopy of the gate electrode has an edge (Inagawa et al., Fig. 16(c) (edge of gate electrode (3(3b)) coincident with layer (2b))), said edge being disposed at a predetermined distance (Inagawa et al., Fig. 16(c) (distance between edge of gate electrode (3(3b)) coincident with layer (2b) and edge of trench opening (see Fig. 16(c)))) from an edge of an opening of the trench,

wherein the predetermined distance (Inagawa et al., Fig. 16(c) (distance between edge of gate electrode (3(3b)) coincident with layer (2b) and edge of trench opening (see Fig. 16(c)))) is predetermined not to prevent the source region (Inagawa et al., Fig. 16(c) (6)) from forming (Inagawa et al., Col. 11, Lines 59-60).

Regarding claim 9, Aoki et al., Jin et al., Yu et al., Currie et al. and Inagawa et al. disclose the method according to claim 1, wherein the device includes a cell region (Inagawa et al, Fig. 2 (area containing transistor cells (Q))) and a gate lead wire region (Inagawa et al., Fig. 2 (area containing gate line (3GL)), wherein the cell region

(Inagawa et al, Fig. 2 (area containing transistor cells (Q))) includes a plurality of cells (Inagawa et al, Fig. 2 (Q)), each of which works as a transistor (Inagawa et al., Col. 6, Lines 6-14), and wherein the gate lead wire region (Inagawa et al., Fig. 2 (area containing gate line (3GL)) includes a gate lead wire (Inagawa et al, Fig. 2 (3GL)) (Inagawa et al., Col. 6, Lines 59-60).

Regarding claim 10, Aoki et al., Jin et al., Yu et al., Currie et al. and Inagawa et al. disclose the method according to claim 9, wherein the transistor (Inagawa et al, Fig. 2 (Q)) (Inagawa et al., Col. 6, Lines 6-14) is an N channel type MOSFET, a P channel type MOSFET or an IGBT (Aoki et al., Col. 2, Lines 44-47).

Regarding claim 14, Aoki et al., Jin et al., Yu et al., Currie et al. and Inagawa et al. disclose the method according to claim 13, further comprising the step of:

forming a source region (Aoki et al., Fig 2B, (4)) having a contact surface between the source region and the substrate (Aoki et al., Fig. 2B, (contact surface is bottom surface of source region (4))), which is disposed near the trench (Aoki et al., Fig. 2B (6)) and is almost parallel to the substrate (see Fig. 2B),

wherein the conductive film (Aoki et al., Fig. 2H (8)) in the trench provides a gate electrode (Aoki et al., Col. 4, Lines 26-28),

wherein the gate electrode (Inagawa et al., Fig. 16(c) (3(3b))) includes a canopy for covering the upper oxide film so that the gate electrode has a T-shaped cross section (Inagawa et al., Fig. 16(c)),

wherein the canopy of the gate electrode has an edge (Inagawa et al., Fig. 16(c) (edge of gate electrode (3(3b)) coincident with layer (2b))), said edge being disposed at a predetermined distance (Inagawa et al., Fig. 16(c) (distance between edge of gate electrode (3(3b)) coincident with layer (2b) and edge of trench opening (see Fig. 16(c)))) from an edge of an opening of the trench,

wherein the predetermined distance (Inagawa et al., Fig. 16(c) (distance between edge of gate electrode (3(3b)) coincident with layer (2b) and edge of trench opening (see Fig. 16(c)))) is predetermined not to prevent the source region (Inagawa et al., Fig. 16(c) (6)) from forming (Inagawa et al., Col. 11, Lines 59-60).

4. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Aoki et al., Jin et al., Yu et al., Currie et al., Inagawa et al. and further in view of Pan et al. (U.S. Patent # 6159781).

Regarding claim 15, Aoki et al., Jin et al., Yu et al., Currie et al., and Inagawa et al. disclose the method according to claim 14, but fail to disclose the distance between the edge of the canopy and the edge of the opening of the trench being, specifically, in a range between 0.05 micrometers and 0.1 micrometers.

It would have been obvious to one of ordinary skill in the art to cause the distance between the edge of the canopy and the edge of the opening of the trench to be in a range between .05 micrometers and .1 micrometers. The claim to the specified range in the distance between the edge of the canopy and the edge of the opening on the trench constitutes an optimization of ranges. *In re Huang*, 100 F.3d 135, 40 USPQ2d 1685, 1688 (Fed. Cir. 1996). The ordinary artisan would have been motivated to modify Aoki et al., Jin et al., Yu et al., Currie et al., and Inagawa et al. in the above manner for the purpose of decreasing gate capacitance (Pan et al., Col. 1, Lines 35-40).

5. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Aoki et al., Jin et al., Yu et al. and Currie et al., and further in view of Poplevine (U.S. Patent # 6218866).

Regarding claim 12, Aoki et al., Jin et al., Yu et al. and Currie et al. disclose the method according to claim 11, and the annealing temperature being 1200 degrees Celsius, but fail to disclose the temperature at which the thermal diffusion process is performed or the annealing temperature in the step of annealing being higher than the process temperature in the step of performing the thermal diffusion process.

Poplevine et al. teaches the formation of a well region wherein a thermal diffusion process with a process temperature of 900-1150 degrees Celsius is employed (Poplevine et al., Col. 8, Lines 8-22).

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the process temperature of the thermal diffusion process of

Poplevine et al. into the method of Aoki et al., Jin et al., Yu et al. and Currie et al. The ordinary artisan would have been motivated to modify Aoki et al., Jin et al., Yu et al. and Currie et al. in the above manner for the purpose of knowing at what temperature to perform the thermal diffusion.

6. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Aoki et al., Jin et al., Yu et al. and Currie et al. and further in view of Narwankar et al. (U.S. Patent # 6218300).

Regarding claim 16, Aoki et al., Jin et al., Yu et al. and Currie et al. disclose the method according to claim 11, but fail to disclose the substrate being annealed in an inert gas atmosphere in the step of annealing.

Narwankar et al. teaches a method of annealing wherein an inert gas is included in the anneal gas stream (Narwankar et al., Col. 6, Lines 30-35)

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the inert gas method of Narwankar et al. into the method of Aoki et al., Jin et al., Yu et al. and Currie et al. The ordinary artisan would have been motivated to modify Aoki et al., Jin et al., Yu et al. and Currie et al. in the above manner for the purpose of preventing recombination of the active atomic species (Narwankar et al., Col. 6, Lines 30-35).

Response to Arguments

7. Applicant's arguments with respect to Henley et al. have been considered but are moot in view of the new ground(s) of rejection.

Applicant argues that the combination of Aoki and Jin is improper. Examiner notes that these arguments are moot in view of the new rejection's reliance on step 516 (Fig. 5A of Jin et al.) instead of step 524 (Fig. 5A of Jin et al.) for the step of annealing.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The cited art discloses similar semiconductor devices.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to William Kraig whose telephone number is 571-272-8660. The examiner can normally be reached on Mon-Fri 7:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ken Parker can be reached on 571-272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

WFK
3/16/2007

SPE Kenneth Parker